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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,945	02/04/2004	Peter J. Fricke	200310842-1	5316
22879	7590	02/15/2006		EXAMINER
				NADAV, ORI
			ART UNIT	PAPER NUMBER
				2811

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/772,945	FRICKE ET AL. <i>file</i>
	Examiner Ori Nadav	Art Unit 2811

— The MAILING DATE of this communication appears on the cover sheet with the correspondence address —
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 02 December 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-6,8-33 and 36-57 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) _____ is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There is no support in the elected embodiment of figure 3 for a silicon-rich insulator of each memory cell is electrically isolated from the silicon-rich insulators of all other memory cells, as recited in claim 4.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 26-33, 38-41, 47-49 and 55-57 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of forming a storage layer and forming a layer of silicon-rich insulator, as recited in claims

26, 38, 47 and 55, are unclear as to the structural relationship between the storage layer, the layer of silicon-rich insulator, and the memory cell.

The claimed limitations of a second conductive layer being at least partially aligned with the middle electrode, as recited in claims 47 and 55, and memory cells of each set being at least partially aligned vertically with each other, as recited in claim 30, are unclear as to whether the second conductive layer is aligned or not aligned with the middle electrode, and how two elements can be partially aligned.

The claimed limitation of forming a second interlayer dielectric layer, as recited in claims 47 and 55, is unclear as to the structural relationship between the second interlayer dielectric layer and the memory cell.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 11, 16 and 58-59 are rejected under 35 U.S.C. 102(b) as being anticipated by Lancaster et al. (5,656,837).

Lancaster et al. teach in figures 8-13 and related text a memory array comprising:

a) a multiplicity of row conductors 166 and a multiplicity of column conductors 160, the row conductors and column conductors being arranged to cross at cross-points, and

b) a two-terminal 160, 166 memory cell disposed at each cross-point, each memory cell having a storage element and a control element coupled in series between a row conductor and a column conductor, and each control element including a silicon-rich oxide insulator 165 (column 14, lines 1-10).

Regarding claim 11, Lancaster et al. teach in figures 8-13 and related text a row conductors are arranged in mutually orthogonal relationship with the column conductors.

Regarding claim 16, Lancaster et al. teach in figures 8-13 and related text a memory cell disposed at each cross-point, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, and each means for controlling including a silicon-rich insulator.

Regarding claims 58-59, Lancaster et al. teach in figures 8 the two terminals of the two terminal memory cell disposed at each cross-point comprise the row conductor and column conductor respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-6, 8-10, 26-33, 38-41, 47-49 and 55-59, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lancaster et al.

Regarding claim 4, Lancaster et al. teach in figures 8-13 and related text substantially the entire claimed structure, as applied to claim 1 above, except stating that the silicon-rich insulator of each memory cell is electrically isolated from the silicon-rich insulators of all other memory cells. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a silicon-rich insulator of each memory cell being electrically isolated from the silicon-rich insulators of all other memory cells in Lancaster et al.'s device in order to use the device in an application which requires various types of storage elements.

Regarding claims 5-6 and 8-10, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a control element of each memory cell comprises a tunnel junction, and the storage element of each memory cell comprises an anti-fuse, a fuse, a tunnel junction, a state-change layer, a chalcogenide,

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in Lancaster et al.'s device in order to use known memory control and storage elements, of which official notice is taken.

Regarding claim 26, Lancaster et al. teach in figures 8-13 and related text substantially the entire claimed structure, as applied to claim 1 above, including a tunnel-junction layer over the silicon rich insulator (since layer 165 is a multilayer) and a second conductive layer 166 over the tunnel-junction layer.

Lancaster et al. do not state that the memory cell is formed by a method of

- b) depositing and patterning a first conductive layer over the substrate, and
- c) forming and patterning a second conductive layer,

However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 38, Lancaster et al. teach in figures 8-13 and related text substantially the entire claimed structure, as applied to claims 1 and 26 above, including a first interlayer dielectric over the storage layer (since layer 165 is a multilayer), and having an opening (see figure 10) through the first interlayer dielectric and extending to the storage layer, and having a conductive material therein as a middle electrode (this conductive material is one of the conductive layers in figure 8, different from the first and second conductive layers, since the array comprises plurality of conductive layers).

This conductive layer, as depicted in figure 10, is contiguous with the storage layer.

Lancaster et al. do not state that the memory cell is formed by a method of

- b) depositing and patterning a first conductive layer over the substrate, and
- c) forming and patterning a second conductive layer,
- d) forming and patterning first and second interlayer dielectrics over the storage layer,
- e) forming an opening through the first interlayer dielectric and extending to the storage layer,
- g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode.

However, these process limitations would not carry patentable weight in this claim

drawn to a structure, because distinct structure is not necessarily produced.

Regarding claims 30, 47 and 55, Lancaster et al. teach in figures 8-13 and related text substantially the entire claimed structure, as applied to claims 1, 26-27 and 38 above, except stating that a second interlayer dielectric is formed over the storage layer,

forming vias as required though the second interlayer dielectric to selectively interconnect memory cells of the memory arrays, wherein the memory cell is formed by a method of

- b) depositing and patterning a first conductive layer over the substrate, and
- c) forming and patterning a second conductive layer,
- d) forming and patterning first and second interlayer dielectrics over the storage layer,
- e) forming an opening through the first interlayer dielectric and extending to the storage layer,
- g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode.
- k) forming vias as required though the second interlayer dielectric, and repeating steps b) through k) until a desired number of memory array layers have been formed.

However, these process limitations would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Lancaster et al. teach in figure 2 a device comprising plurality of cells and decoders. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a second interlayer dielectric over the storage layer and to form vias as required though the second interlayer dielectric to selectively interconnect memory cells of the memory arrays, in Lancaster et al.'s device in order to prevent short circuits and in order to provide connections between the various cells and parts of the device, respectively.

Regarding claims 27-29, 31-33, 39-41, 48-49 and 56-57, Lancaster et al. teach a memory array comprising a multiplicity of the memory cells, a substrate carrying electronics and an IC comprising a multilayer memory (see also figure 2), wherein

- a) a multiplicity of the memory arrays are arranged in memory layers,

Response to Arguments

Applicant argues that there is support in page 6, lines 23-29 for a silicon-rich insulator of each memory cell being electrically isolated from the silicon-rich insulators of all other memory cells, as recited in claim 4.

Although page 6, lines 23-29 recites a silicon-rich insulator of each memory cell being electrically isolated from the silicon-rich insulators of all other memory cells, there is no support in the elected embodiment of figure 3 for a silicon-rich insulator of each memory cell is electrically isolated from the silicon-rich insulators of all other memory cells, as recited in claim 4.

Applicant argues that Lancaster et al. do not teach a two-terminal memory cell. Each cell, because of the flash memory array of Lancaster et al. consists of devices having at least three terminals – source, drain, and gate.

The claimed invention recites a memory array comprising a two-terminal memory cell. This phrase does not preclude the device from comprising source, drain, and gate. Furthermore, applicant teaches a memory array in which the two terminals comprise

row conductor 30 and column conductor 40. Lancaster et al. also teach a memory array in which the two terminals comprise row conductor 160 and column conductor 166. Therefore, Lancaster et al. teach a two-terminal memory cell. Each cell, as claimed.

Applicant argues that the examiner did not provide any evidence for the obviousness rejection.

Although the examiner did not provide any evidence for the obviousness rejection, the obviousness was established by using the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



O.N.
2/6/06

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800